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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/566,515 | 01/30/2006 | Pankaj Shrivastava | US03 0254 US2 | 7347 |

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| EXAMINER | |
|---|---|
| KNOLL, CLIFFORD H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2111 | |

| NOTIFICATION DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/566,515 | SHRIVASTAVA ET AL. | |
| | Examiner | Art Unit | |
| | Clifford H. Knoll | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. *Claims 1-7, 11, 13-16, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuhira in view of standard register use, as evidenced by Yoshida (US 5450566 A).*

Regarding claims 1 and 21, Mitsuhira discloses the register bank blocks (e.g., Fig. 1, "36"), the decoder circuit for activating one of the bank blocks (e.g., Fig. 1, "44") where different interrupt event operations result in selecting different ones of the blocks (e.g., col. 4, lines 39-44). Mitsuhira also discloses arithmetic operations (e.g., col. 4, lines 9-12) and registers as used for data processing (e.g., col. 1, lines 10-12), but neglects to expressly mention that register data is commonly used in arithmetic operations; however, Examiner takes Official Notice that it is commonplace to perform arithmetic operations on register data, as evidenced by Yoshida (e.g., col. 4, lines 45-48). It would have been obvious to one of ordinary skill in the art to combine register contents with the arithmetic operations of Mitsuhira, because use of registers allows for enhancements, such as efficient use of register addressing modes.

Regarding claim 2, Mitsuhira also discloses the execution of the first program stream, and executing the second stream associated with an interrupt event (e.g., col. 6, lines 4-9).

Regarding claim 3, Mitsuhira also discloses the second program stream has higher priority than the first (e.g., col. 5, lines 35-40).

Regarding claims 4 and 5, Mitsuhira also discloses multiplexing the input data bus by receiving a register bank selection signal coupling the activated register bank block to the input data bus (e.g., col. 6, lines 5-7).

Regarding claims 6 and 7, Mitsuhira also discloses multiplexing the output data bus by receiving a register bank selection signal coupling the activated register bank block to the output data bus (e.g., col. 6, lines 7-9).

Regarding claim 11, Mitsuhira also discloses first and second bank blocks are currently enabled and independently addressable (e.g., col. 4, lines 51-54).

Regarding claim 13, Mitsuhira discloses the register bank blocks (e.g., Fig. 1, "36"), the decoder circuit for activating one of the bank blocks (e.g., Fig. 1, "44"), receiving and determining if an interrupt is to be fulfilled (e.g., col. 6, lines 4-9), and if so selecting a second block isolated from the first ones of the blocks (e.g., col. 4, lines 39-44). Mitsuhira also discloses arithmetic operations (e.g., col. 4, lines 9-12) and registers as used for data processing (e.g., col. 1, lines 10-12), but neglects to expressly mention that register data is commonly used in arithmetic operations; however, Examiner takes Official Notice that it is commonplace to perform arithmetic operations on register data, as evidenced by Yoshida (e.g., col. 4, lines 45-48). It would have been obvious to one

of ordinary skill in the art to combine register contents with the arithmetic operations of Mitsuhira, because use of registers allows for enhancements, such as efficient use of register addressing modes.

Regarding claim 14, Mitsuhira also discloses the execution of the first program stream, and executing the second stream (e.g., col. 6, lines 4-9).

Regarding claim 15, Mitsuhira also discloses the second program stream has higher priority than the first (e.g., col. 5, lines 35-40).

Regarding claim 16, Mitsuhira also discloses the processor (e.g., Fig. 1, "16").

Regarding claim 19, Mitsuhira also discloses the memory circuit with program stream data (e.g., Fig. 1, "28").

Regarding claim 20, Mitsuhira also discloses instructions for storing and restoring register bank block contents (e.g., col. 6, line 67 – col. 7, lines 10).

2. *Claims 8-10 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuhira and standard register use, as applied supra, in view of Fujimura (US 5751988 A).*

Regarding claim 8, Mitsuhira neglects to expressly mention returning from an interrupt and the need to restore existing conditions; however, this is widely known as seen in Fujimura (e.g., col. 2, lines 45-49). It would have been obvious to one of ordinary skill in the art to combine Fujimura with Mitsuhira because Fujimura teaches a means to return to the register bank block selection that was interrupted in order to continue operating upon completion of the higher priority processing.

Regarding claim 9, Mitsuhira also discloses the switching is based on priority (e.g., col. 5, lines 35-40). Fujimura teaches the storing upon interrupt (e.g., col. 2, lines 28-32).

Regarding claim 10, Mitsuhira also discloses the bank signal is solely based on interrupt priority (e.g., col. 5, lines 34-37, all conditions listed considered a prioritization of signal).

Regarding claim 17, Mitsuhira also discloses selecting the first register block (e.g., col. 5, lines 35-37), halting execution of the second program stream (e.g., col. 16, lines 18-21), but does not expressly mention resuming execution of the first program stream; however this is widely known as seen in Fujimura (e.g., col. 2, lines 45-49). It would have been obvious to one of ordinary skill in the art to combine Fujimura with Mitsuhira because Fujimura teaches a means to return to the register bank block selection that was interrupted in order to continue operating upon completion of the higher priority processing.

Regarding claim 18, Mitsuhira also discloses executing the second program stream does not alter contents of the first register bank block in suspended use (e.g., col. 6, lines 1-3).

3. *Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuhira and standard register use, as applied supra, in view of standard debugging techniques, as evidenced by Hohl (US 6035422 A).*

Regarding claim 12, Mitsuhira also discloses a register for access to a plurality of bank blocks (e.g., col. 4, lines 51-54), but neglects to mention a step of debugging; however, Examiner takes Official Notice it is widely known to access all register data during debugging as evidenced by Hohl (e.g., col. 34, lines 62-64). It would have been obvious to one of ordinary skill in the art to combine widely known debug techniques to Mitsuhira because providing full access to operational data during debug maximizes the amount of information to bear on a problem that is being debugged.

### *Response to Arguments*

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Clifford H Knoll/
Clifford H Knoll
Patent Examiner
Art Unit 2111

chk